The effect of sintering temperature on the development of grain boundary traps in zinc oxide based varistors

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A series of zinc oxide based varistors containing 0.5 wt% Bi_2O_3 and 0.5 wt% Mn_2O_3 was prepared by a conventional mixed oxide route and sintered at temperatures between 950° and 1300°C. All samples showed varistor behaviour, although as the sintering temperature was increased from 950°C to 1300°C, the non-linearity coefficient, α, decreased from 22 to 3.

Deep level transient spectroscopy of the varistors showed that the main active electron trap migrated to shallower levels within the bandgap as the sintering temperature increased. At the lowest sintering temperature, where α attained the highest values, a second, shallower trap was also activated.

1. Introduction

Zinc oxide based varistors are characterised by highly non-ohmic current-voltage behaviour and, due to their high current handling capability, are commonly used as protective elements against high-voltage transients in electrical circuits [1, 2]. The non-ohmic properties are controlled by the behaviour of electrostatic grain boundary barriers that prevent electrons from crossing into adjacent grains at low applied voltages and cause the material to behave in an insulating manner. At higher voltages the ceramic becomes highly conducting due to the depression of the interface charge by minority carrier holes that are generated by impact ionisation by 'hot' electrons [3, 4].

Models describing the structure of varistor grain boundaries are broadly divided into homojunction [5] and heterojunction [6] types. Both of these invoke band-bending in the grain boundary regions due to the filling of electron traps, whose formation and densities are associated with the incorporation of specific dopants. The structure, and consequently the varistor properties of the electrostatic barrier can be fine-tuned by the introduction of specific metal oxide additives, such as bismuth, manganese and cobalt oxides.

Deep level transient spectroscopy (DLTS) is an experimental technique that has long been used to characterise trap states in semiconductors [7] and has also been applied in numerous studies to investigate zinc oxide based systems, including varistors [8–14].

Most DLTS studies of varistors to date have focussed on linking the energy and density of traps to variations in the levels of specific dopants in order to understand their origin and effect. For example, Fan and Freer [8] studied the effects of silver and aluminium doping in varistors sintered at 1180°C. They found traps at ca. 0.15 and ca. 0.25 eV below the conduction band edge that increased in density with aluminium doping and decreased with silver doping, associating the shallower trap with the non-linear behaviour and the deeper trap with varistor stability during breakdown. Similar trap energies have been reported in other varistor systems [12–14], suggesting that these traps are due to intrinsic defects, and that their activation and density are controlled by the addition of specific dopants. An additional trap has been reported at ca. 1.0 eV below the conduction band edge in one study and is attributed specifically to interface states formed by lattice interaction with segregating oxides [14].

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In single crystal semiconductors, DLTS is performed by observing thermal emission from majority carrier traps at deep states in a depletion region, which is created below a surface Schottky contact by applying a reverse bias. By pulsing the applied bias the traps are filled repeatedly. The emission rate of each peak is measured as a function of temperature, often using a 'double box car' system. From this it is possible to calculate the energy difference between the trap level and the conduction or valence band edge. Since the geometry of the test sample is well defined, the height of the DLTS peaks can also be used to calculate the trap concentration.

DLTS studies of single crystal ZnO have used a similar sample geometry, in which a surface Au electrode is applied to form a Schottky contact with the zinc oxide [9, 10]. Under these conditions, trap filling is assumed to occur near to the surface of the ZnO, just below the Au contact, within the depletion region formed by the reverse biasing of this junction.

Varistors are polycrystalline materials in which the traps of interest for their special properties are associated with the grain boundary regions. Hence it is essential to ensure that such traps are activated during measurement. By analogy with the single crystal process, DLTS measurements made on polycrystalline materials using the same contact geometry will result in the filling of grain boundary traps just below the Schottky contact. However, since varistor grain boundaries themselves behave as back-to-back Schottky barriers, those grain boundaries lying largely perpendicular to the field direction should also be affected by the applied bias and undergo trap filling. Thus many grain boundary regions within the varistor will be cycled to some extent during measurement, resulting in uncertainty in the total area and the extent over which trap activation is taking place within the sample. Consequently, only limited data about the traps can be extracted: in fact, from these measurements, whilst it is possible to calculate trap energies, it is not possible to establish reliably absolute trap concentrations without making assumptions about the extent of the active region. Nevertheless with careful measurement it is still possible to make valid comparisons between the densities of traps in the same sample if more than one peak is visible.

Varistor performance is very sensitive to processing, with variations of a few 10's of degrees in the peak sintering temperature, giving rise to significant differences in electrical performance [15]. Since these differences are associated with changes in the behaviour of the electrostatic grain boundary barriers, it is possible that sintering conditions also influence both the densities and the number of active traps associated with the barriers: something that has not been studied systematically to date. However, there are also likely to be complex interactions between the effects of differing dopants in typical varistor formulations and in such situations the attribution of a specific trap energy to the effects of a particular dopant may not be feasible.

In this contribution we report the results of a study of the effect of sintering temperature on trap formation and activation in a simplified varistor formulation by comparing the DLTS spectra of samples sintered at temperatures between 950°C and 1300°C.

2. Experimental method

A simplified varistor based on zinc oxide doped with 0.5 wt% Bi_2O_3 and 0.5 wt% Mn_2O_3 was prepared by a standard mixed oxide route. Compacts 10 mm diameter and 2 mm thick were formed by uniaxial pressing at 170 MPa and sintered at temperatures between 950°C and 1300°C for two hours in air using heating and cooling rates of 100°C h^{-1}. Sintered densities were estimated from measurements of sample weights and dimensions. Polished surfaces were prepared for SEM analysis by grinding a flat face on SiC paper and polishing with diamond paste, prior to mounting on insulating stubs for observation in a Phillips XL30 FEGSEM.

Current-voltage measurements were carried out on the bulk samples using an adjustable DC voltage source (Brandenberg 475R) and current meter. The non-linear exponent, α, was determined for each sample from I-V plots using current densities of 0.1 mA cm^{-2} and 1 mA cm^{-2} according to the equation:

$$\alpha = \log(J_2/J_1)/\log(E_2/E_1) \quad (1)$$

where E_1 and E_2 represent the electrical fields across the sample at current densities J_1 and J_2.

DLTS was carried out using a system based on a Bio-Rad Polaron DL4600 with a modified Boonton 72B capacitance meter and a continuous flow liquid nitrogen cryostat. Evaporated gold contacts were made to both top (1 mm diameter dots) and bottom (planar electrode) surfaces of the varistor. The fill pulse applied to the samples was 70% of the breakdown voltage of the varistor. Heating was via an integral heater, and the temperature was measured using a platinum resistance thermometer. Spectra were acquired by scanning over the temperature range 80–300 K, using a scan rate of 0.2 K s^{-1}. The rate window settings were between 200 s^{-1} and 4 s^{-1}.

3. Results and discussion

Fig. 1 shows backscattered electron images of polished sections of the varistors. In all samples, the density was between 90% and 95% of theoretical. Within the microstructure of the 950°C sintered sample (Fig. 1a) a distributed bismuth rich phase is clearly visible as bright patches at the zinc oxide grain boundaries, predominantly located at triple points. In the sample sintered at 1000°C (Fig. 1b) some bismuth rich phase appears to have spread out from the triple points and extended along a few grain boundaries during sintering, where it now sits as small isolated islands (arrowed). Some localised grain growth has occurred. At sintering temperatures of 1100°C and above

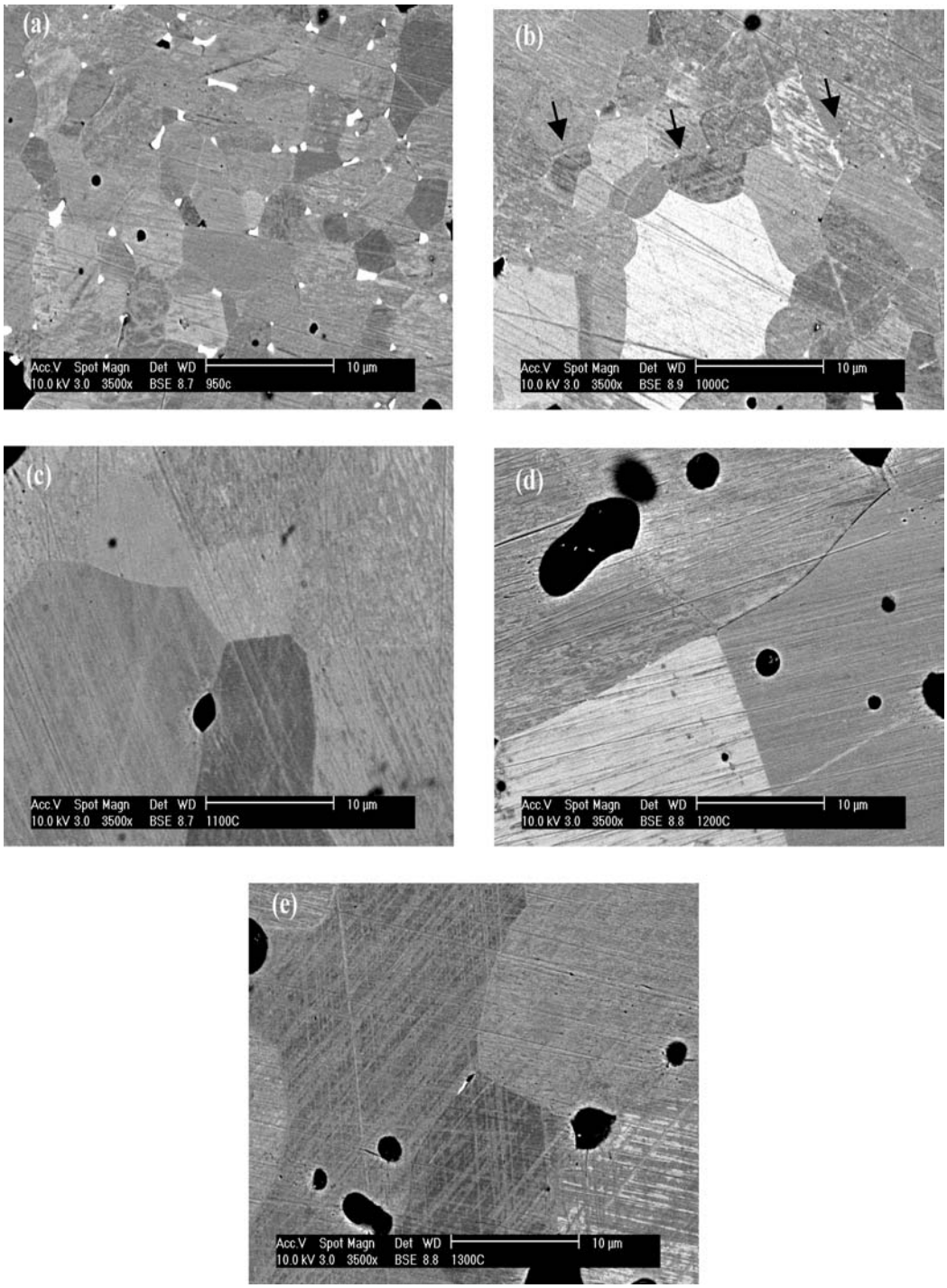

Figure 1 Backscattered electron images showing the effect of variations in sintering temperature on the distribution of Bi-rich phases present in the samples sintered at (a) 950°C, (b) 1000°C, (c) 1100°C, (d) 1200°C, (e) 1300°C. Scale bar = 10 μm.

(Fig. 1c–e), considerable grain growth has occurred and a bismuth rich grain boundary phase is not generally visible except as small isolated pockets, suggesting that significant dopant volatilisation has occurred at these temperatures. There is thus a steady change in grain boundary microstructure with increasing sintering temperature. At the lowest sintering temperatures most of the bismuth rich phase is located at triple points. As the temperature increases there is evidence of increased wetting at grain boundaries, while at the highest temperatures, where extensive grain growth has occurred, there is significant bismuth loss due to volatilisation. Since the varistor effect requires the presence of bismuth at the grain boundaries, these changes in microstructure are likely to be reflected in differences in varistor behaviour and hence the electrical structure of the grain boundary regions. Fig. 2 shows the variation of the non-linear coefficient, α, with sintering temperature. α reaches a peak value of 22 for a sintering

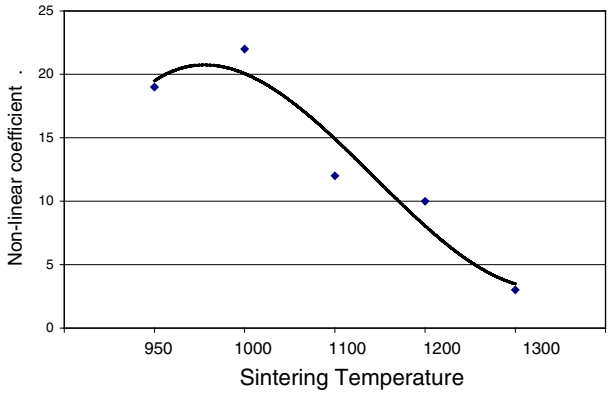

Figure 2 Variation of the non-linear coefficient, α, with sintering temperature.

temperature of 1000°C, corresponding to the temperature at which wetting of the grain boundaries is first observed. As the sintering temperature is increased further there is a progressive reduction in α, with the 1300°C sample showing only a weak varistor effect.

For the samples sintered between 950°C and 1200°C the breakdown voltage per grain boundary fell in the range 4.0 ± 0.5 V, which is consistent with other reported values [2]. For the 1300°C sintered sample, however, the breakdown voltage per grain boundary was 0.5 V, an anomalously low value for which the most likely explanation is the presence of a high proportion of inactive interfaces due to the loss of varistor forming dopants by volatilisation at this high sintering temperature.

Three of the varistor samples, namely those sintered at 950°C, 1100°C and 1300°C, were characterised further by DLTS analysis. Fig. 3a–c show representative DLTS spectra, collected from each of the samples. The different curves in each figure correspond to the data being collected through rate windows of 200 s^{-1}, 50 s^{-1} and 50 s^{-1}. Two peaks, indicating two active traps, were found in the spectra from the sample sintered at 950°C (Fig. 3a), whereas only a single peak was observed in the samples sintered at 1100°C (Fig. 3b) and 1300°C (Fig. 3c). Arrhenius plots of T^2/e against $10^3/T$ were generated for each of the traps, from which their levels in the bandgap could be calculated (Fig. 4). The traps in the sample sintered at 950°C were found to lie 281 meV and 173 meV below the conduction band edge, the trap in the sample sintered at 1100°C lies 235 meV below the conduction band edge and the trap in the sample sintered at 1300°C lies 214 meV below the conduction band edge.

The deeper trap observed in the 950°C sample and the traps in the 1100°C and 1300°C samples fall within the range of energies reported in the literature for the L_2 trap [13], and has been attributed to the presence of zinc interstitials, with low trap densities being associated with varistor instability. Although, for the reasons described earlier, it is not possible to say reliably whether the trap density changes with sintering temperature, we can note

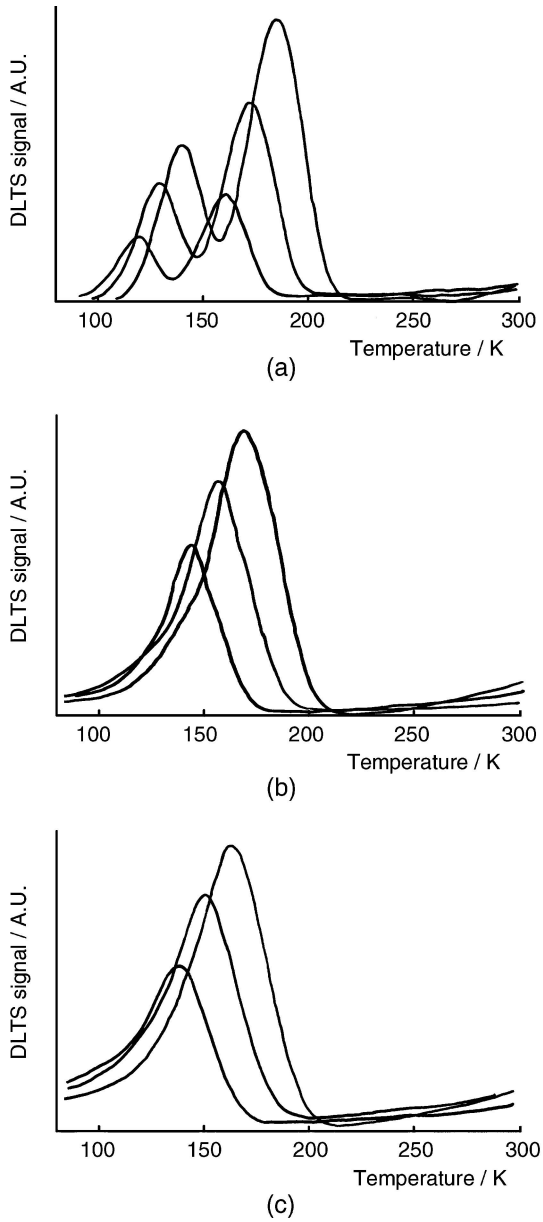

Figure 3 DLTS spectra of samples sintered at (a) 950°C, (b) 1100°C, (c) 1300°C, using rate windows of 200 s^{-1}, 50 s^{-1} and 10 s^{-1}.

that as the sintering temperature is increased from 950° to 1300°C this trap becomes shallower. Lower sintering temperatures and higher α values are therefore associated in this study with the trap occupying a deeper level. Such differences in trap energy with sintering temperature, although previously unreported, are not surprising, and are likely to be related to changes in the local environment of the dopant. The breadth of the DLTS peaks from this trap at each sintering temperature suggests that it occupies a spread of energies, which are likely to be associated with small changes in the immediate neighbourhood of the active defect. The reduction in the peak heights of the traps at lower emission rates is characteristic of incomplete trap filling, which also suggests that the trap has the form of an extended defect. Changes in sintering temperature are likely to result in broader changes in trap environment,

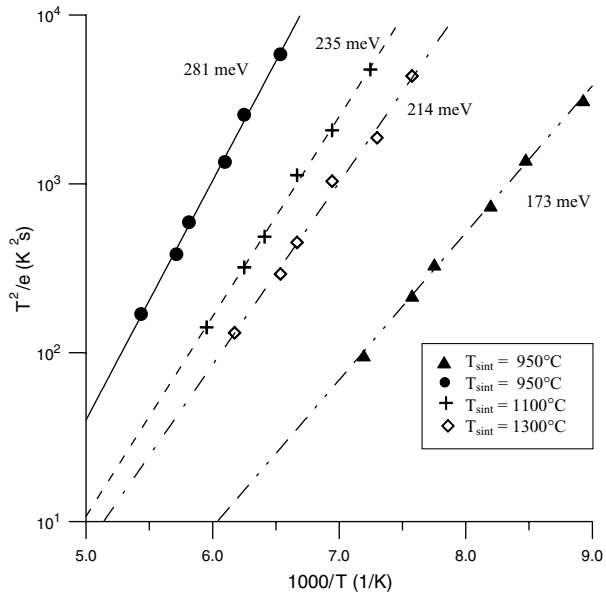

Figure 4 DLTS data plotted as T^2/e against 1000/T.

causing the trap energies to become centred on a different mean value, both through modifications to local atomic structure and broader differences in microstructure due to changes in the form of the intergranular, bismuth rich phase. The observed differences in trap energy with sintering temperature may also account for the broad range of levels reported (0.2–0.3 eV) for this defect in other studies.

In the sample sintered at 950°C the second trap has an energy that is within the range reported for the L_1 trap [8]. This second activated trap has a lower density than the L_2 trap in the 950°C sample. It is associated with the varistor showing the highest value of α and is not observed in the samples sintered at higher temperatures. This trap has been linked with high levels of varistor non-linearity and is attributed to the effect of structure modifications by defects introduced through donor additions [8]. The observation that this trap is only present in the sample showing the highest non-linearity is consistent with these reports. However its absence in samples that are nominally of the same composition, but which were sintered at higher temperatures suggests that it is not simply related to the presence of appropriate dopants, but to their incorporation in specific ways, conducive to varistor formation, within the microstructure.

4. Conclusions

A series of zinc oxide based varistors containing 0.5 wt% Bi_2O_3 and 0.5 wt% Mn_2O_3 was prepared by a conventional mixed oxide route and sintered at temperatures between 950°C and 1300°C. All samples showed varistor behaviour, with a peak α value of 22, occurring at a sintering temperature of 1000°C.

DLTS measurements showed the presence of a single trap in the samples sintered at 1100°C and 1300°C, two traps found in sample annealed at 950°C. From the Arrhenius plot, this appears to be due to a distribution of deep levels associated with a single trap that moves deeper into the bandgap as the sintering temperature decreases. A second electron trap also operates in the sample annealed at 950°C.

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